Dynamic MOS circuits for Neuromorphic Hardware Implementation Based on the Paradigm of Activity

Shinji, Karasawa
Miyagi National College of Technology.
Medeshima, Natori-shi, Miyagi, 981-1239 Japan
E-mail: karasawa@miyagi-ct.ac.jp

ABSTRACT

A system of neuromorphic hardware implementation is realized by utilizing traditional technologies of dynamic MOS circuits where a decoder as a substitution of neuron is formed by means of a subset of impulses as substitutions of a subset of activities. The decoder translates from many activities to one activity and that is the fundamental element of an intelligent hardware where a subset of electric charges are used as a representative of a unit of activity and a floating MOSFET is used as a programmable contact. A subset of bi-directional connecting points of a decoder can be used as the connecting points of the encoder possessing of the same pattern of activities. That is, an efferent route can be used as the afferent route by exchanging a signal source and the load. In this paper, dynamic MOS circuits for an interpreter are presented as an example to demonstrate remarkable advantages of the paradigm of activity for the intelligent hardware implementation.

Keywords: Brain mechanism, Programmable logic device, Impulse, Decoder, Digital signal translator, Dynamic MOS IC.

1. INTRODUCTION

Most of traditional intelligent systems are computational [1],[2]. The computational system has a great benefit of duplication. Although a computing system is a powerful tool to share the intelligence, every affair in the real world is renewed and it possesses some identities. Now, an automatically renewable interface is desired for a today's computer.

On the other hand, the activity of a neuron is discrete and a unit of activity itself does not include plural information processing. The author proposed the paradigm of activity for a design methodology of intelligent device where an impulse results in a digital change of a state and the meanings of activity belong to the cell [3]. An impulse is a substitution of a unit activity and an address decoder operates the function of neuron [4]. This type of device functions by means of transferring of activities. The data flow in this system does not need a tag. The simplicity of impulse driven circuit system makes possible to realize the plasticity that yields extensible performances [5].

A kind of address decoder is used as a logic circuit in the activity transfer system. The logic of decoder is as follows. When the preconditions are satisfied, it outputs an action. A pattern of the functioning can be copied to the connecting points of an address decoder. The address decoder with pass transistor is able to control the stream of activities. Supervision of processes for hardware implementation is carried out by this mechanism.

A decoder can be formed in a dynamic MOS (Metal Oxide Semiconductor). In the field of PLD (Programmable Logic Device), a medium of programmable nonvolatile memory is achieved by means of a kind of floating gate MOSFET (FG-MOSFET). The FG- MOSFET is used as a memory in a flash memory, but it is also used as a connecting element in a PLD [6]. Now, PLD is developing as a PPL (Path Programmable Logic) [7] and a NOR type of Flash memory [8].

The paradigm of activity widens the applications of traditional dynamic MOS technology. An intermittent bi-directional flow of electric current can be considered as an intermittent bi-directional flow of activities. A subset of connections of a decoder is able to use as the connections of the encoder. This mechanism is available to automatic implementation of intelligence in a dynamic MOS IC.

The conventional design technology of "a finite-state machine" in the field of VLSI design technology [9] is utilized for the activity transfer circuits as "a finite action transfer machine". The intelligent system of activity transfer device is simple compared with traditional information processing.

In this report, the paradigm of activity for the brain mechanism and dynamic MOS circuits for neuromorphic hardware implementation are discussed. In order to clarify the design process of the impulse driven networks, a hardware system of interpreter was described as an example for architecture of intelligent device.

2. A STRATEGY OF PROGRAMMABLE DECODERS TO EMULATE THE BRAIN MECHANISM

Architecture of activity transfer system

The junctions and address decoders are necessary for the transference of activity. The set of input terminals of an address decoder corresponds to the set of traffic permission conditions of an individual route. The address decoder functions automatically by means of a set of serial impulses through a shift register. A decoder with pass transistor is able to control to form an additional circuit where the decoder selects a set of activities at the junction.

Forming of circuit is carried out during transferring of activities where a set of impulses on an array of delay elements becomes a set of paralleling inputs. An output of decoder is able to ignite the other agent or it is able to suppress the other activities. This additional agent is able to control the other stream of activities.

Since an agent manipulated by one decoder, plural sets of activities are decoded by means of layered decoders. A component has the wider use than the whole, but the combination has the wider diversity than the component. The combination of components brings the adaptability. Then, the activities are organized.

An output of decoder can be held in the loop through rounding [10]. A rounding activity in a loop is a kind of short-term

memory on the activity. By using activities of these loops, a decoder in an upper layer decodes a set of plural components. The decoder together with short-term memories is able to organize subsets of activities.
There are segmentations between subsets of activities. A command signal to construct a layered structure of decoders is ignited when a subset of activities become a blank. By this segmentation, an impulse is outputted from a decoder on the subset. So, the output of an impulse represents a set of components.
On the other hand, outputs from many controllers are connected to an input terminal of actuator. These connections are OR logic. As one of a method to realize OR operation, a negative impulse is produced when any positive impulse does not come. This OR connections are realized by means of NAND connections for inverted signal according to De Morgan's theorems. This circuit was inspired from the nerve circuit of the cerebellum [11].

An impulse as a substitution of discrete activity

The simplest agent is a reflex agent. The shape of one action becomes an impulse. It disappears without stopping at a stationary state. The action varies every moment and it is nonlinear. An activity is expressed by using a delta function.
The result of a unit of activity is a change of a digital state. A discrete activity is written by an if-then-rule (a production rule [12]), written as “If preconditions are satisfied, then it initiates the action assigned”. An agent is expressed by means of the program in the field of traditional artificial intelligence.
Any way, an activity is the change of state. The activity is able to create the circuit that replays the same activity. In a brain, functioning points coincide with the connecting points of neuron i.e. decoder. The formed decoder executes one reaction.
An automatic implementation of decoder can be designed according to transmission of a set of discrete activities, where a subset of serially sampled impulses transmitted along a line of delay elements are placed side by side in parallel lines.
A transmitting impulse along a line of delay element provides a timing signal. The timing signal together with functioning signal of impulse is able to control the serial activities. The decoder decodes a timing signal together with the set of present state of activities.
The decoder with pass transistor is able to carry out to control the other stream of activities. Such system is achieved by the additional implementation without changing the established structure. This extensible system makes possible to develop towards more sophisticated performance.
A combinational logic is presented by means of a logical formula of sum-of-product. A circuit for the agent is composed of OR circuit of AND circuit. Here, AND connections are implemented by means of the activities of preconditions. OR connections for the serial controller are realized by means of connectable elements.
Although the points of connections correspond at the points of high level of original signal at reading, FG-MOSFET is programmed through injection of hot electron by using high level of gate voltage. This programming due to the injection of electron yields disconnection. So, an automatic implementation of decoder is carried out by using inverted signal, and the non-inverted signal is used for a reading operation.

Circuits for control of serial activities

A continuous clock signal is obtained from an oscillator. A ring oscillator made of looped inverters of odd number generates signal continuously. A counter together with a clock signal is able to provide a timing signal.
Since the impedance of n-MOS inverter is very high, a stray capacitance holds the voltage. MOS inverters connected in a line operates as a shift register where the movement of data can be controlled by a clock signal.
Two-phase clock signals are able to control the transmission of impulses in a dynamic MOS network. For an example, clock signals of F1 and F2 are switched between zero and V_{DD}. Each clock signal has the same period, and the high times are somewhat shorter than the low times in order to have non-overlapping at high times.
The operation of a line of paired dynamic MOS inverters by applying alternately two-phase signals is able to transmit a sequence of impulses. This circuit operates the function of a serial-in/parallel-out register. The register distributes paralleling outputs to address decoders and it will be also used to implement a new decoder. The shift register for this purpose needs some driving power. A ratio type of dynamic MOS shift register is able to provide driving power.

A programmable and controllable connecting element

A stacked gate avalanche injection MOS (SAMOS) disconnects by means of channel hot electrons [13]. The FG-MOSFET consists of a dual-stacked poly-silicon structure in which the bottom gate is floating. The thin oxide isolates the floating gate from the drain. The thin oxide provides an injection area for hot electrons. The tunneling of electrons from the drain to the floating gate takes place by the channel hot electron mechanism owing to the electric field in the channel between source and drain. The electron energy distribution presents a tail in the higher energy side that can be modulated by the longitudinal electric field of top gate.
When we implement the circuit by utilizing the injection of hot electrons, the treatment results in cutting of the line. Since an activity ignites an impulse, the hot electron is injected by means of the inverted signal i.e. that of inactivity.
The floating gate MOS FET (e.g. NOR Flash memory cell) is erased by Fowler-Neordheim tunneling effect of the oxide. The tunneling current flows from floating gate to silicon surface, where a strong electric field induces a quantum-mechanical phenomenon of tunneling without destroying its dielectric properties [14]. This current of ejection is very little compared with injection.
A combinational logic circuit is made of pull-down transistors and a pull-up transistor. In order to construct a decoder automatically, floating gate transistors are used as pull-down transistors. Since the high level of threshold voltage on the control gate makes possible disconnect state of the floating gate transistor, every input signal is divided into double lines where one is non-inverted and the other is inverted. One of a pair is low level necessarily and it is able to keep connectable state.
The output of the decoder will keep high level when every pull-down transistor is disconnection. If one of pull-down transistor connects the output to low level, the output becomes low level. The output of decoder never keeps high level but every connectable pull-down transistor is the state of disconnection. That is, every line with a low level of gate voltage at implementation remains as a connectable state and the connectable transistor cuts the current between source and drain at the low level of gate voltage.
This NOR type of decoder will output a high level when every connectable transistor is the state of disconnection. By insertion

of an inverter in front of every input terminal of programmable NOR circuit, an AND plane of a PLA (Programmable Logic Array) is realized.

3. AUTOMATIC IMPLEMENTATION OF A DIGITAL SIGNAL TRANSLATOR

Strategy of a hardware implementation of intelligence

An action of decision-making is ignited by means of a decoder in which many input lines are connected to one output line. A command line for an execution is connected to many output lines. A decoder connects from many input lines to one output line. An encoder connects from one input line to many output lines. The circuit that made of a decoder and an encoder is able to carry out every intelligent activity, for this circuit covers the logic of every activity.

Since the drain and the source in FG-MOSFET is exchangeable symmetry, it functions as a controllable passive element. A FG-MOSFET is able to operate as a programmable and controllable bi-directional connection. The intermittent current is able to transmit electric charges toward both directions.

The bi-directional logic circuit transmits a subset of electric charges from drain to source. By switching from input line to output line and from output line to input line, the some amount of electric charges are able to transmit reverse direction through this connection.

A logical relationship is represented by the connections from input to output. The meaning of transference of subset of electric charges by means of an intermittent current depends on the device connected to those terminals. A bi-directional logic circuit is realized by means of this charge transfer circuit.

A programmable bi-directional digital signal translator

Implementation of a decoder possessed of an encoder: A bi-directional digital signal translator is composed of a pair of bi-directional decoders. That is, one bi-directional decoder is implemented by using inputting digital signal and another bi-directional decoder is implemented by using outputting digital signal on the same item and the connection between these two outputs forms a bi-directional digital signal translator.

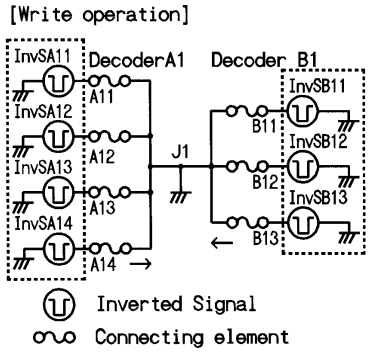


Fig.1 Write operation of a bi-directional decoder possessed of encoder

Fig.1 illustrates a circuit for write operation of a bi-directional digital signal translator. A pair decoders A and B those are made of bi-directional connections is able to exchange the pattern of digital signal A and that of B by connecting those outputs. The operation of each bi-directional digital signal translator is assigned by the selection signal via the gate of a FG-MOSFET.

Bi-directional digital signal translator: Since the input possesses some electric power and the output is passive, a decoder is able to use as the encoder by exchanging the inputs and the output. By making use of bi-directional connections, a pattern of connections is able to transfer the activities from many terminals to one terminal, or it is also able to transfer the activity from one terminal to many terminals.

By using the same plural points of programmable bi-directional connections, a bi-directional decoder is changed to the encoder by the switching where the output terminals of a decoder are switched to input terminals of the encoder and an input terminal of a decoder is switched to the output terminal of the encoder.

AND logic function of the bi-directional decoder is realized by means of internal resistances inserted in the route of H level of the signal sources, where L level of the signal sources are connected to the common ground directly. If one of signal source is connected to the low level (L) directly, AND logic operation is achieved by means of the resistance of high level of the other signal source. Here, if any of signal sources become (L) level, the voltage of J point becomes (L) level.

On the other hand, OR logic function of bi-directional encoder is conducted by means of high impedance of load resistances.

A decoder functioned of AND logic makes decision from the constituents. An encoder functioned of OR logic makes outputs according to the decision of decoder connected. So, the decoder possessed of encoder carries out the intelligent agent.

Fig.2 and Fig.3 illustrate the operation of bi-directional digital signal translator. The direction of digital signal translation by means of the circuit shown in Fig.2 is opposite compared with that of Fig.3.The former illustrates an afferent route and the latter illustrates an efferent route.

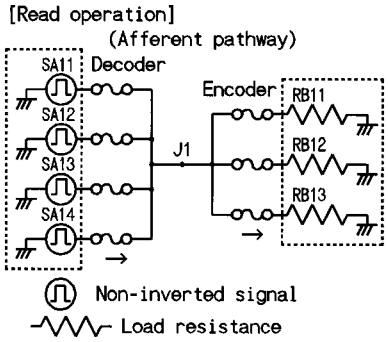


Fig.2 The afferent route of a bi-directional digital signal translator

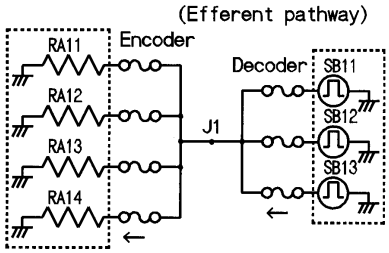


Fig.3The efferent route of a bi-directional digital signal translator

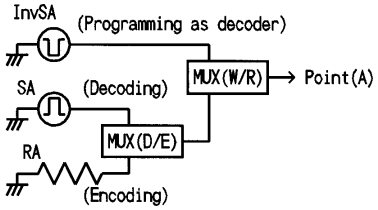
MOS Circuits for a programmable bi-directional digital signal translator

Switching of connections on a bi-directional translator: The operation of a bi-directional digital signal translator is changed by means of a switching of the connections. Table 1 shows the connections of the points (A), (B) and (J).

Table 1 Switching of the connections on a bi-directional translator

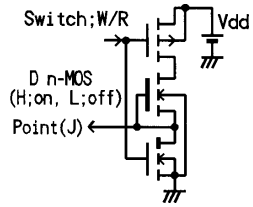
operation \ point		A	B	J
Write		InvSA	InvSB	GND
Read	afferent	SA	load	float
	efferent	load	SB	float

Switching circuit on a connecting element: A combination of transmission gates is used for the switching of connections on point (A) or point (B). The switching circuit for the terminal of bi-directional element (A) or (B) is shown in Fig.4



F.g.4 The switching circuit connected to a bi-directional element

The switching circuit that is connected to J point: Fig.5 illustrates the switching circuit that is connected to the junction (J1) between a decoder (1) and encoder (1). The switching at the floating point of the junction is achieved by a p-MOPSFET and a n-MOSFET in a series. D n-MOSFET is used to provide the current for the encoder.



*D n-MOS is a depletion type of n-channel MOSFET that is normally ON and OFF state is achieved by lowering the gate voltage.

Fig.5 A switching circuit possessed of a supplier of current

By using the circuit shown in Fig.5, the point (J) is connected to Vdd at reading operation, but it is connected to GND at writing operation. Moreover this circuit supplies electric current at the (H) level of J point.

Switching operations by means of dynamic MOS circuit: The combination of transmission gates is used for changing of the routes [15]. The circuit that is shown in Fig.6 outputs inverted signal or non-inverted signal according to a command. At a writing operation, the gate of p-MOS FET (P3),(P4),(P5) is low level (ON) and the gate of n-MOS FET (N3),(N4),(N5) is high level (ON) but the gate of p-MOS FET (P1),(P2) is OFF and the gate of n-MOS FET(N1)(N2) is OFF.

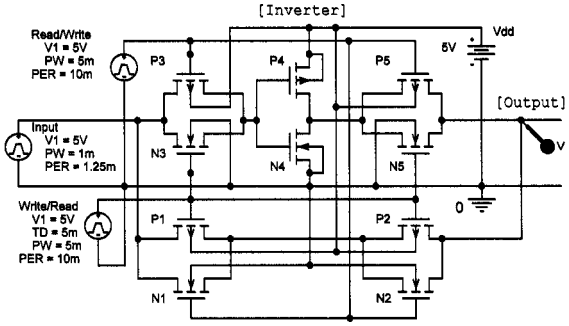
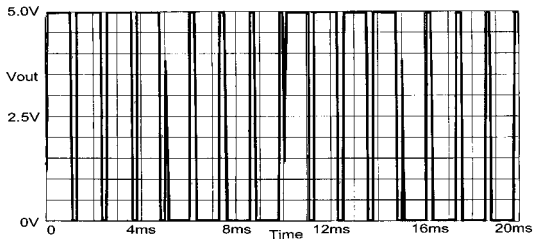


Fig.6 A switching circuit to exchange between the inverted signal and the non-inverted signal.

A result of computer simulation: Fig.7 shows the output on the MOS circuit shown in Fig.6. These data are obtained by using a computer simulator PSpice [16]. The circuit inverts the outputting signal alternately. Fig.7 indicates the existence of a spike at the end of switching. This spike is caused by a storage effect of capacitance. The problem will be solved by means of the timing of impulsive operations.



Fi.g7 Responses on a switching circuit shown in Fig.6

There are many data and techniques for VLSI that is made of traditional elements. The technologies in the field of dynamic MOS VLSI are available for the bi-directional logic circuit. But, the practical design of a FG-MOSFET needs some data those depend on the process of fabrication.

4. SPECIFICATIONS OF APPLICATIONS

Specification of linguistic activities

A nerve system controls a behavior by means of discrete activities. A decoder transforms a set of discrete activities into one impulse, and an encoder disassembles it into a sheet of impulses. Although the nerves connected to a vocal organ to utter are different to the nerves connected with the auditory sensors, the segmentations for a layered structure of linguistic activities is the same. Although, the speech recognition is achieved by means of digital signal processing such as Hidden Markov models (HMM), the concept of activity is useful for the specification of programmable decoders for linguistic activities [17], [18], [19].

A pattern of frequency components of the speech voice reflects the activities of vocal tract. The signals those are abstracted by means of an auditory nerve system become intermittent. The

speech understanding is carried out by means of a series of discrete activities. These activities are represented by means of phonetic alphabets. Data on the segmentation of linguistic activities is important for the implementation of programmable decoders.

Since every activity is composed of impulses in a nerve system, a complex affair is expressed by means of layered structure of activities. The output of decoder on a phoneme is kept in a short-term memory and a word decoder decodes a set of phonemes. The output of decoder on a word is kept in a short-term memory of a sentence and a decoder of sentence decodes the set of words. The output of an impulse sent to a short-term memory of the sentence.

The output is sent to a memory in an upper layer. The register in an upper layered is able to arrange subsets of activities. The output is sent back to the register in order to refresh, because the activity of short-term memory must be suppressed when it is unnecessary.

The linguistic expressions are processed by means of existing decoders if it does not need to create a new decoder. The network is constructed with the extension method where the function of network is extended by means of inserting a new decoder into the existing system.

[Application Ⅰ]

Media of archiver: The bi-directional translator exchanges two kinds of expressions mutually. The function is available as a media of archiver. As examples, it is able to translate from an array of characters on a word to a registered number of the word. Also the circuit is able to use to translate from an array of registered number of words of a sentence to a registered number of the sentence.

A serial activity is able to load to a register according to the occurrences systematically where the timing of shift is given by the signal of segmentation. There are plural layers in linguistic activities. There are the layer between an array of characters on a word and a registered number of the word, and the layer between an array of registered number of words of a sentence and registered number of the sentence. In general, a register possessed of the bi-directional digital signal translator is available to manipulate a subset of activities.

[Application Ⅱ]

Interpreter: A bi-directional translation is carried out by means of two kinds of expressions on the same affair. Since one sentence can be expressed by means of a serial series of symbols by using a layer structure of registers possessed of bi-directional logic circuits, the linkage of two kind of linguistic expression makes possible to translate between two serial series of symbols.

[ApplicationⅢ]

Bi-directional translator between a visual pattern and a linguistic expression: The translation from visual pattern into a linguistic expression is achieved by means of the bi-directional translator where the output of bi-directional decoders on a visual pattern and the output of bi-directional decoder on the linguistic expression are connected. In the case that components of the activity are organized, a decoder for vision or a decoder for linguistic expression becomes a layered structure.

Here, the normalization of data those are adjusted by the numbers of picture elements helps recognition of visual pattern. There are a great number of things and affairs in a view field. A target of visual recognition is divided by means of its characteristics such as color, and the pattern of target can be recognized by means of a bi-directional decoder.

Since the wiring between the register and paralleling decoders is fixed, the number of picture elements of templates and the number of picture elements on every divided target must be adjusted. The total number of connecting points coincides to that of distributing lines. The number of inputs on a decoder has to coincide with that on a pattern of target. The original visual data on a target must be translated automatically from by fixed calculations accompanying with this normalization. Here, the space data on a target such as center, maximum point, and minimum point are used for a normalization of the data on vision

5. NUMERICAL EXAMPLES

Programmable bi-directional logic circuits for linguistic use

The VLSI that translates between a series of alphabetic symbols on a word and a registered number of the word can be used as an archive of words.

There are 50～60 kinds of phonetic signs. 64 kinds of phonetic signs are distinguished by means of 6 bits signal. If one alphabetic symbol is expressed by means of 8 bits signal and a word is expressed by means of 16 alphabets tentatively, a word is distinguished by means of 8×16=128 bits data. Here, we assume that 8,192 kinds of words are distinguished by means of 13 bits signal. In this case, the quantity of connecting points of 128×8,192 =1,048,576 points for input side will be necessary.

On the other hand, the quantity of points for registered number side will be 13×8,192=106,496. This VLSI possessed of these connecting points is able to use as the medium of words.

VLSI that translates between a subset of registered numbers on words and the registered number of one sentence can be used as an archive of the sentences. If one sentence is expressed with the data of 13 bits and a sentence is expressed with 19 words tentatively, a sentence is distinguished by means of 13×19=247 bits data. The 13 bits of registered number on each sentence is implemented as a decoder and those connecting points are used as an encoder.

If 247 bits of data distinguish 8,192 kinds of words, the quantity of connecting points will be points 247×8,192 =2,023,424 for the word data side and the quantity of 13×8,192=106,496 for registered number side.

An example on programmable bi-directional logic circuit for a vision

Since the wiring between a register and paralleling decoders is fixed by means of the connections, the data on every target must be adjusted to the data bus.

If we assume the number of data bus is 256 lines for a picture of length for 16 segments and side for 16 segments, and 24 of bits is used for the information of each picture element, 256×24=6,144 bits are necessary for each pattern. Here, the value of 24 bits is 8 bits for each 3 primary colors. The total quantity of connections for 1,000 pieces of templates will be 6,1444,000.

The decoder that is mode of programmable bi-directional connecting points is able to produces output instantaneously at the data matching. The autonomous type of device is able to realize by means of today's technologies of VLSI.

6. CONCLUSIONS

In this report, an automatic implementation of intelligent hardware was discussed from the paradigm of activity and some circuits made of dynamic MOS circuits were presented.

The intelligent activity of human consists of biochemical reactions. The connections of each neuron are different, every neuron represents different agent. The nerve system is not always a device of information processing.

The activity transfer device can be termed as "the impulse driven device". One reaction is expressed by an if-then-rule. That is, "if preconditions are satisfied, then it operates the function". This discrete reaction is expressed by a sum-of-product expression in Boolean algebra.

Technologies of dynamic MOS network and technologies of PLD can be utilized for the activity transfer system, because existence of the functioning is represented by the existence of electric charge. Since a hardware system is able to function always, impulse driven system is able to realize by means of MOS circuits. The design technology of "state machine" in VLSI is available for the impulse driven device.

The impulse driven system does not need data stored. Since each impulse is transferred intermittently, it is possible to transfer the activity bi-directionally in the network. We can term the system that transfers discrete activities as "impulse driven device" in order to distinguish from traditional digital circuits.

The trace of transmission of activities is memorized as the connecting points. The transference of activities results in junctions and address decoders. The decoder can be formed by means of a PLD. The organized activities are able to memorize in the layered decoders.

The sequential operations of a network of layered decoders for the forming of impulse transfer route can be designed by using the clock. The time divided control by using multiple-phase of clock makes possible to form the layered circuits.

The author considers that the paradigm of activity will open a new promising field of hardware intelligence, because the impulse driven VLSI system is able to realize by using existing technologies.

The interface that is designed by the concept of activity will contribute to decrease the gap between the activities in a brain and the traditional information processing.

Moreover, the paradigm of activity in a nerve system will provide deeper understanding of the brain mechanism as follows. The linguistic expression is able to summarize the information as one concept. The linguistic expression is incorporated to the superstructure of intelligence and it plays the important roles in a brain.

Although the meanings of linguistic expression depend on the community, the hardware system that understands speech will be a layered structure of impulse driven circuits. Since the nerve system is constructed in the real world and it is affected from the real world, there is the common feature that comes from the real world.

It is considered that an electronic device will be able to operate a part of the function of human brain. But it is difficult to make the electronic device that possesses the same function of a human brain. The author hopes that this new paradigm of activity will contribute to the development of science and technology of intelligence.

7. REFERENCES

[1] J. P. Levy, D. Bairaktaris, J. A. Bullinaria, P. Cairns, **Connectionist Models of Memory and Language**, UCL Press Limited, 1995.

[2] R. J. Schalkoff, **Artificial neural networks**, McGraw-Hill Book Co. 1997.

[3] S. Karasawa, "Decoder for neuron translation models for brain mechanisms", **Research Reports; Miyagi National College\ of Technology,** pp.19-25, 2000.

[4] S. Karasawa, "A communicating real-time decision-making machine", **Proceedings of Mlnet familiarization workshop on learning robots, Learning in monitoring and supervision multi-agent systems,** Heraklion, Crete, April, 1995.

[5] S. Karasawa, "Impulse driven electronic device", **Japan patent number 3496065,** Application number 2000-179115**,** Filing date May 11, 2000.

[6] R. L. Geiger, P. E. Allen, N. R. Strader, **VLSI design techniques for analog and digital circuits**, McGRAW-Hill, pp.826, 1990.

[7] J. Gu, K. F. Smith, "A structured approach for VLSI circuit design", **Computer**, pp.9-22, Nov., 1989.

[8] H. Motta, G. Ragone, O. Khouri, G. Torelli, R. Micheloni, "High-voltage management in single-supply CHE NOR-type flash memory", pp.554-568, **Proc. IEEE,** Vol.91, No.4, 2003.

[9] C. Mead, L. Conway, **Introduction to VLSI Systems**, Addison-Wesley, pp.82, 1980.

[10] S. Karasawa, "Impulse recurrent loops for short-term memory which merges with experience and long-term memory," **Proc. of 3rd Int. Conf. on Cognitive and Neural systems,** pp.36, Boston Univ., May 26-29, 1999.

[11] S. Karasawa, J. Oomori, "Impulse circuits for a distributed control inspired by the neuroanatomical structure of a cerebellum," **Intelligent engineering systems through artificial neural networks**, Vol.10, pp.185-190, ASME press, New York, 2000.

[12] A. Newell, H. Simon, **Human Problem Solving**, Prentice Hall, Englewood Cliffs, NJ. 1972.

[13] D. Kahng, S. M. Sze, "A floating gate and its application to memory devices", **Bell Syst. Tech.J**., 46, 1283, 1967.

[14] M. Lenslinger, E. H. Snow, "Fowler-Nordheim tunneling into thermally grown SiO_2", **J. Appl. Phys,** Vol.40, pp.278-283, 1969.

[15] N.H.E. Weste, K. Eshraghian, **Principles of CMOS VLSI Design: A Systems Perspective**, AT&T, 1985.

[16] PSpice A/D Basics, **Schematic Design Entry OrCAD Capuure, OrCAD**, Cedence Design Systems, Inc., 2001.

[17] S. Karasawa, "Neuronal Models for speech processing", **Proc. of Inter. Conf. of Speech Processing,** Seoul National. Univ., Korea, pp.103-108, Aug. 1999.

[18] S. Karasawa, "Neuromorphic impulse circuits for a speech production",**7th Western Pacific Regional Acoustics Conference**, Kumamoto, Japan, 3-5 Oct. Vol.1, pp.207-210, 2000.

[19] S. Karasawa, "Model of linguistic activities as ad hoc interactive activities in an impulse driven multi-agent system", **7th World Multi-conference on Systemics, Cybernetics and Informatics,** Orlando, USA, July 27-30, Vol.14, pp.365-370, 2003.